Chapter VII:

Interface scavenging

In this chapter, the scavenging concept is analyzed. As it was commented in the introduction, Kim *et al.* [1] explored this effect for the first time with the aim of reducing the SiO_x layer that growth at the high κ/silicon interface. The interlayer (IL) scavenging is produced by the decomposition of the SiO_x [1-3]. The reduction in thickness of this SiO_x layer, that is a low κ material, decreases the total EOT.

Several works have studied the scavenging effect using HfO_2 as dielectric [1-8]. Also, ZrO_2 was explored [1]. However, other than the publications from our group [9-12], we have not found any reference for scavenging on other alternative high κ dielectrics deposited on Si.

Here, MIS devices using Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ grown by HPS with the two-step method (presented in the last chapters) were fabricated. The top electrode was Ti (capped with Al or Pt in order to avoid oxidation or nitridation). This metal has been reported in several works as an oxygen scavenger [1,6,8]. The objective of this chapter is to check if the scavenging effect is compatible with these high κ materials to achieve a reduction in the interfacial SiO_x and thus, obtaining a lower EOT while keeping a reasonable interface trap density and leakage current.

Electrical measurements (C-V_{gate} and J-V_{gate} curves) were performed to the MIS capacitors with Ti as top electrode. These results were compared with the same samples with Pt. HRTEM images were obtained in order to study the thickness of the dielectric and the interfacial layers. The conductance method [13] and DLTS [14] measurements were used to obtain the interfacial trap density, D_{it}.

VII.1.- EXPERIMENTAL METHOD

MIS devices with Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ as dielectrics were fabricated by means of HPS with the two-step method introduced in the former chapters. First of all, thin metallic films of Gd, Sc or a nanolaminate of them were deposited during different times at 30 W in an Ar atmosphere. Afterwards, and without breaking the vacuum, an *in situ* plasma oxidation was performed in an Ar/O_2 ambient in order to oxidize the metallic layer. The *rf* power and the duration of this step were different for each sample. Both processes were carried out, in all the cases, at room temperature and at a pressure of 0.50 mbar.

Various thicknesses of Ti (capped with Al or Pt) were e-beam evaporated as the top electrode. The backside of the wafers was covered with 50 nm of Ti / 100 nm of Al. Several forming gas anneals (FGAs) were performed at different temperatures. Besides, Pt samples were fabricated in order to have a reference and check the differences.

VII.2.- RESULTS AND DISCUSSION

2.1.- Thick Ti layers as top electrode with Gd_2O_3

In this section, the objective was to study the compatibility of the scavenging effect with plasma oxidized Gd_2O_3 films. MIS devices were fabricated without field oxide (FOX) and with 80 s of Gd and a plasma oxidation of 300 s (both processes performed at 30 W). The top electrode was a stacked structure formed of 50 nm of Ti capped with 100 nm of Al in order to avoid titanium surface oxidation or nitridation when annealing in forming gas. This sample was similar to the reference one studied in section 2.2 of chapter V with a metallic gate of Pt and here it was used for comparison. Capacitors were measured before and after a FGA at 300 ºC for 20 min.

The C-V_{gate} characteristics measured at 10 kHz for these devices are presented in figure VII.1 for the Pt reference sample (in the left hand side) and the Ti gated MIS devices (right hand side) for the as deposited capacitors (in dashed lines) and after the FGA at 300 ºC (in solid lines). The Pt devices present similar values of the accumulation capacitance before and after the FGA (only a slight decrease of this value is observed after the temperature treatment, which corresponds to a 0.2 nm increase in

the EOT obtained with the algorithm developed by Hauser *et al.* [15]). This was due to an oxide regrowth or Pt adhesion problems, as it was commented in chapter V. Additionally, the hump in depletion observed in the as deposited capacitors disappeared after the FGA, pointing out to an interface improvement due to hydrogen passivation.

For the Ti case, a great increase in the accumulation capacitance is observed for the sample after the FGA. In fact, a reduction of ~1.8 nm of EOT is achieved, reaching an EOT value of 1.7 nm. This rise of the accumulation capacitance value for the Ti gated devices is a consequence of the scavenging effect of Ti, which removes oxygen from the interfacial layer of SiO_x. This effect is even observable for the as grown samples and without any temperature treatment. Comparing the Pt and Ti capacitors before the FGA, it is observed a slightly higher accumulation capacitance for the sample with Ti (thus, around 0.3 nm of EOT lower). The explanation could be that during the Ti e-beam evaporation, some heating of the film by infrared radiation is likely. Although this process is performed in vacuum (~10^{-6} mbar) and the sample is separated around 50 cm from the crucible, the melted Ti is at 1200-1500 ºC and this heat could induce interface scavenging. Definitely, this effect is more remarkable when a

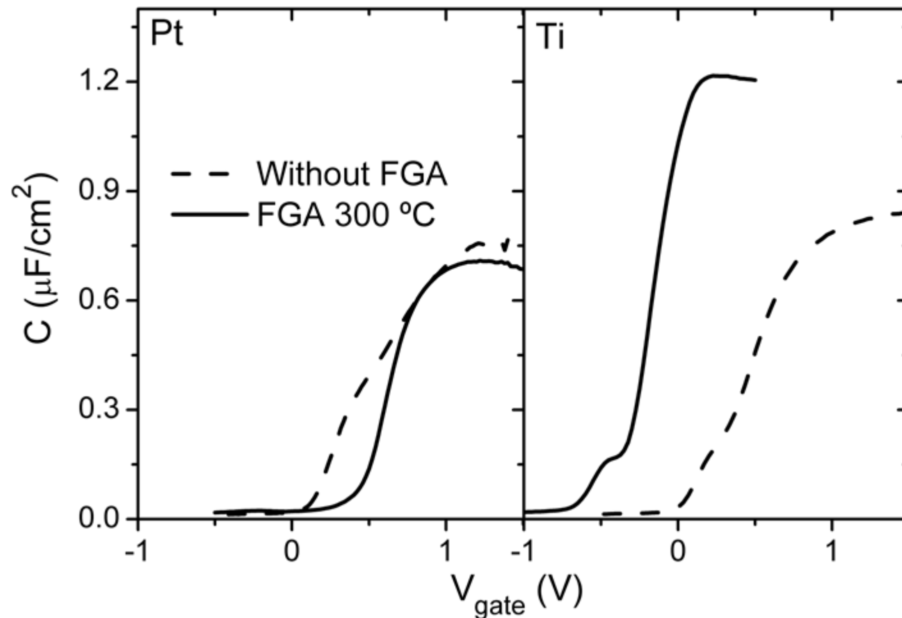

Figure VII.1: C-V_{gate} curves for the sample with 80 s of Gd and a 300 s plasma oxidation at 30 W measured before (dashed lines) and after the FGA at 300 ºC (solid lines) for two different top contacts: Pt/Al (as a reference) and thick Ti/Al.

temperature annealing is performed, as it is observed for the sample after the FGA. This effect was also reported by Nakajima *et al.* [3].

Besides, capacitance curves present a hump for the Ti devices before and also after the FGA, which is caused by a high D_{it} (~2×10^{12} $eV^{-1}cm^{-2}$, about one or two orders of magnitude higher than the Pt sample). These D_{it} values were extracted from the conductance method [13]. This interface degradation, due to the formation of additional Si dangling bond defects, is related to the scavenging effect as it was pointed out by Cerbu *et al.* [16].

To sum up, the EOT and D_{it} values before and after the FGA for both types of metallic contacts are presented in table VII.1.

	Without FGA		FGA 300 ºC	
Metallic contact	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
Pt/Al	3.8	5×10^{12}	4.0	---
Ti/Al	3.5	4×10^{12}	1.7	2×10^{12}

Table VII.1: EOT and D_{it} values extracted from electrical measurements before and after the FGA at 300 ºC for samples with 80 s of Gd and a plasma oxidation of 300 s (at 30 W) with two different top electrodes: Pt/Al and thick Ti/Al. "---" means that the D_{it} value is under the detection limit of the method.

The cross-sectional HRTEM images of these samples after the FGA at 300 °C are shown in figure VII.2 for the two different metal electrodes. Figure VII.2(a) presents the sample with Pt as top metal (as a reference) and figure VII.2(b), the same dielectric film but with a thick Ti layer. As it was commented in chapter V, the pure Pt sample presents 6.1 nm of an amorphous Gd_2O_3 layer on top of 1.8 nm of interfacial SiO_x, probably grown during the long plasma oxidation. On the other hand, when Ti is used as top metal, no SiO_x interface can be observed. This is due to the scavenging effect of Ti. It is also noticeable, that the thickness of the Gd_2O_3 film is ~2.1 nm lower than in the Pt case. This result points out to an excessive scavenging of the thick Ti layer that not only removes oxygen from the SiO_x interface (~1.8 nm), but also scavenges part of the

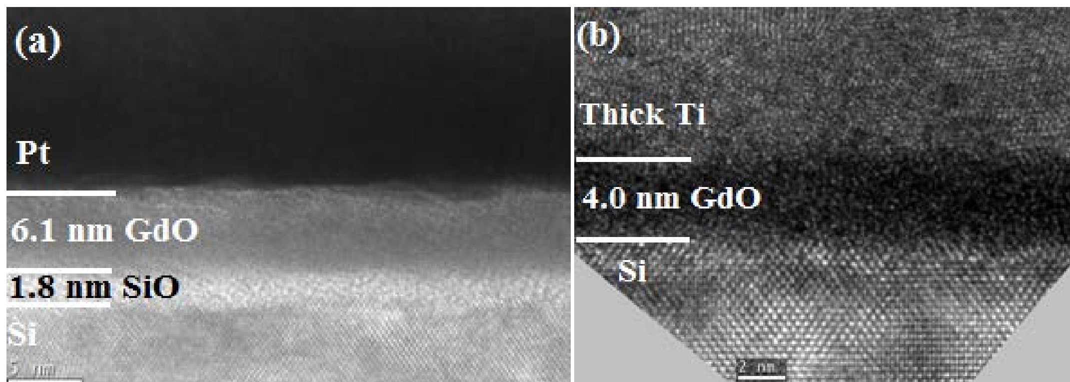

Figure VII.2: HRTEM images for the samples with long oxidation (300 s at 30 W) with two metallic contacts: (a) Pt (as a reference) and (b) thick Ti.

dielectric material (reducing this layer ~2.1 nm). This would produce an increase of the leakage current due to the thinner high κ film, which is not desirable.

Therefore, the main conclusion of this section is that the interface scavenging process works on HPS deposited Gd_2O_3, but needs optimization, since an excessive thickness of the Ti layer, used as top electrode, implies a reduction of the IL but also a degradation of the dielectric film, reducing its thickness after the FGA. Thus, a second set of samples with thinner Ti films was fabricated, with the aim of controlling the scavenging effect produced.

2.2.- Optimization of the scavenging effect for plasma oxidized Gd_2O_3

To optimize the scavenging effect, a second set of samples with a softer oxidation (less duration and lower *rf* power) together with a thinner Ti films was fabricated. MIS capacitors with FOX were grown with 80 s of Gd and a plasma oxidation at 20 W during 100 s. These were the best conditions obtained in chapter V for Gd_2O_3. Since the metallic Gd deposition time is the same as in the first section, it can be assumed that the Gd_2O_3 thickness is similar, around 6.1 nm. On the other hand, it is expected a thinner interface since it was used a less aggressive oxidation. Different thicknesses of Ti were used as top electrode: 2.5, 5 and 17 nm (all capped with 25 nm of Pt). The objective was the decrease of the interfacial SiO_x thickness without degrading the G_2dO_3 layer. Several FGAs at 300, 350 and 400 ºC were performed during 20 min and the devices were measured before and after the different FGAs.

Figure VII.3 depicts the normalized C-V_{gate} characteristics of these samples with different thicknesses of Ti, measured at 10 kHz before and after the FGAs. All the samples present a characteristic hump in depletion in the C-V_{gate} curve before the temperature annealing due to a high D_{it} value. This hump was also observed for the Pt sample used as reference (shown in section 2.3 of chapter V).

For the sample with 2.5 nm of Ti (figure VII.3(a)) and after the annealings, there is a slight increase of the accumulation capacitance. Besides, there are no relevant differences between the several temperatures of the FGAs. Then, the scavenging effect of the 2.5 nm Ti film is moderate and saturates for an annealing temperature of 300 °C. Furthermore, the FGAs make the C-V_{gate} fall more abruptly and the hump in depletion disappears, which indicates an improvement in the oxide/semiconductor interface.

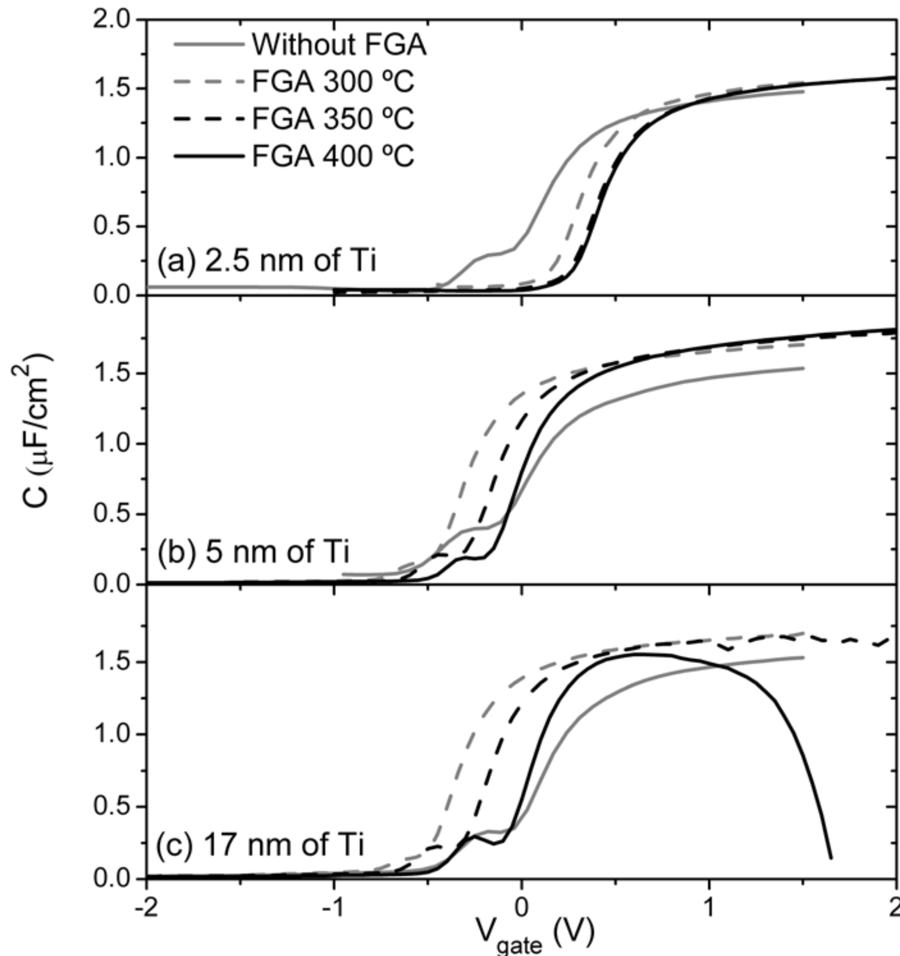

Figure VII.3: C-V_{gate} curves for the sample with 80 s of Gd and an 100 s plasma oxidation at 20 W measured before and after several FGAs with different thickness of Ti layers: (a) 2.5 nm, (b) 5 nm and (c) 17 nm.

For the 5 nm Ti devices (in figure VII.3(b)), the accumulation capacitance value visibly increases after the FGA at 300 ºC. No significant differences can be noticed for higher FGAs at 350 and 400 °C for this sample. In this case, the scavenging saturation occurs for the FGA at 350 °C. For this Ti thickness, the distortion of the curve in depletion is reduced after annealing, but it is still clearly observed a hump, even after the FGA at 400 ºC. This points out to a high D_{it} due to the scavenging effect, as it was commented in the former section.

For the thicker Ti layer with around 17 nm (figure VII.3(c)), the behavior of the C-V_{gate} curves is similar to the former sample up to an annealing temperature of 350 °C, but for annealing temperatures above 400 °C, there is a severe accumulation capacitance drop, pointing out to an excessive scavenging effect. The normalized conductance for this sample presents a value over 1 S/cm^2 for gate voltages higher than 1 V, supporting this aggressive scavenging effect.

The left hand side of figure VII.4 presents the evolution of the EOT value as a function of the annealing temperature for these samples with several Ti thicknesses. It is important to highlight that the Pt sample used as reference, analyzed in chapter V and presented in figure V.23, had an EOT value around 2.2 nm (before and also after the FGAs). For the thinner Ti thickness, there is a hardly noticeable decrease in the EOT

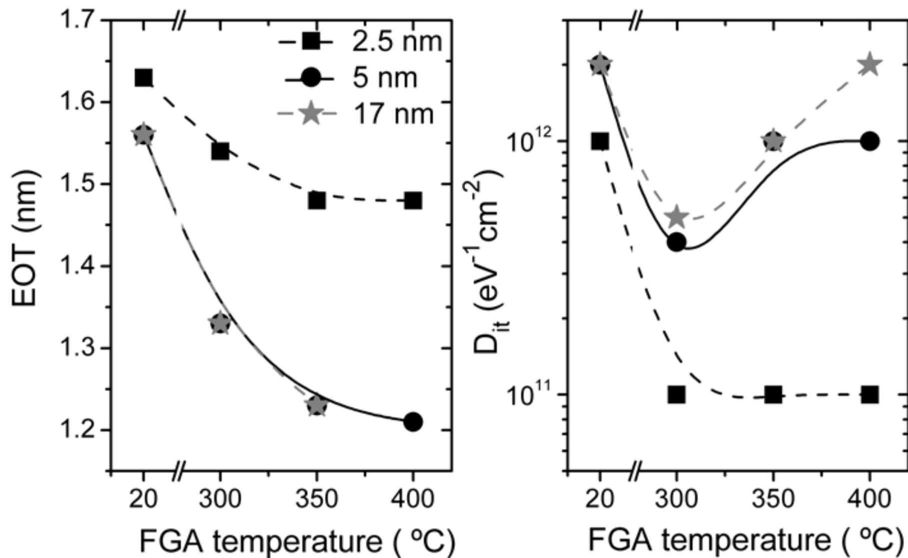

Figure VII.4: EOT (left) and D_{it} (right) values as a function of the annealing temperature for the samples fabricated with different Ti thicknesses: 2.5, 5 and 17 nm.

from a value slightly higher than 1.6 nm (for the as deposited sample) to 1.5 nm (after the FGAs). The saturation effect for this sample discussed before is also noticed in this figure for annealing temperatures above 300 °C. For the sample with 5 nm Ti layer, the EOT reduction goes from a value slightly lower than 1.6 nm (for the as grown sample) to 1.2 nm (after FGA at 400 °C). Finally, for the sample with the thicker Ti top metal layer, the trend in the EOT decrease is the same as the one observed in the previous sample up to the FGA at 350 °C. Due to the capacitance drop observed in figure VII.3(c) after FGA at 400 °C, it is not possible to obtain the EOT value for this temperature. Besides, from figure VII.4, it can be observed that the EOT is similar for all the as deposited samples (around 1.6 nm), but this value is slightly lower for samples with higher Ti thickness. When comparing this value with the EOT of the Pt gated device, it can be concluded that some scavenging takes place even during the deposition of the metal contact, as it was also commented it the former section. Besides, the mild EOT reduction when increasing the Ti thickness is also an indication that during the top contact evaporation there is some scavenging in the samples, most likely due to heating by infrared radiation, as it was pointed out before and also was observed in reference [3].

Additionally, figure VII.4 represents, in the right hand side, the evolution of D_{it} as a function of the annealing temperature for the different Ti thicknesses. In the Pt case, it was observed that the D_{it} decreased around one order of magnitude to ~10^{11} $eV^{-1}cm^{-2}$ after the FGAs. In this case, for the sample with 2.5 nm of Ti, the D_{it} achieves a similar value to that obtained for the Pt sample after the FGA at 300 °C, showing an interface improvement, as was also qualitatively observed in the C-V_{gate} of that sample with the disappearance of the hump in depletion. However, thicker Ti layers show a higher value of the D_{it} even before annealing, which is another confirmation of the scavenging effect during evaporation (lower unannealed EOT means more intensive scavenging, which produces more defects). For these samples, the lowest FGA temperature, 300 °C, produces a reduction of the D_{it} up to 4-5×10^{11} $eV^{-1}cm^{-2}$. These values increase again to the ~10^{12} $eV^{-1}cm^{-2}$ range when the annealing temperature is raised. D_{it} degradation is even more noticeable for the sample with 17 nm of Ti after the FGA at 400 °C, suggesting again that, excessive scavenging results in a defective interface. Other works

have reported similar values of the D_{it} using ZrO_2 [17], single crystalline Gd_2O_3 [18] and polycrystalline Gd_2O_3 with an amorphous GdSiO layer [19].

In figure VII.5, the leakage current density is represented as a function of the gate voltage. These results are in agreement with the capacitance measurements (shown in figure VII.3). The leakage of the sample with 2.5 nm of Ti does not change before and after FGAs, with a value around 10^{-6} A/cm^2 at 1 V (figure VII.5(a)). This means that only a negligible scavenging is happening. Analogous results were obtained for the reference sample with Pt presented in chapter V. For the sample with 5 nm of Ti, current density increases moderately as the annealing temperature is raised. In any case, leakage current is in the order of 10^{-4} A/cm^2 at 1 V for all the FGAs (figure VII.5(b)), similar to those reported in previous works [17,20]. On the other hand, for the sample

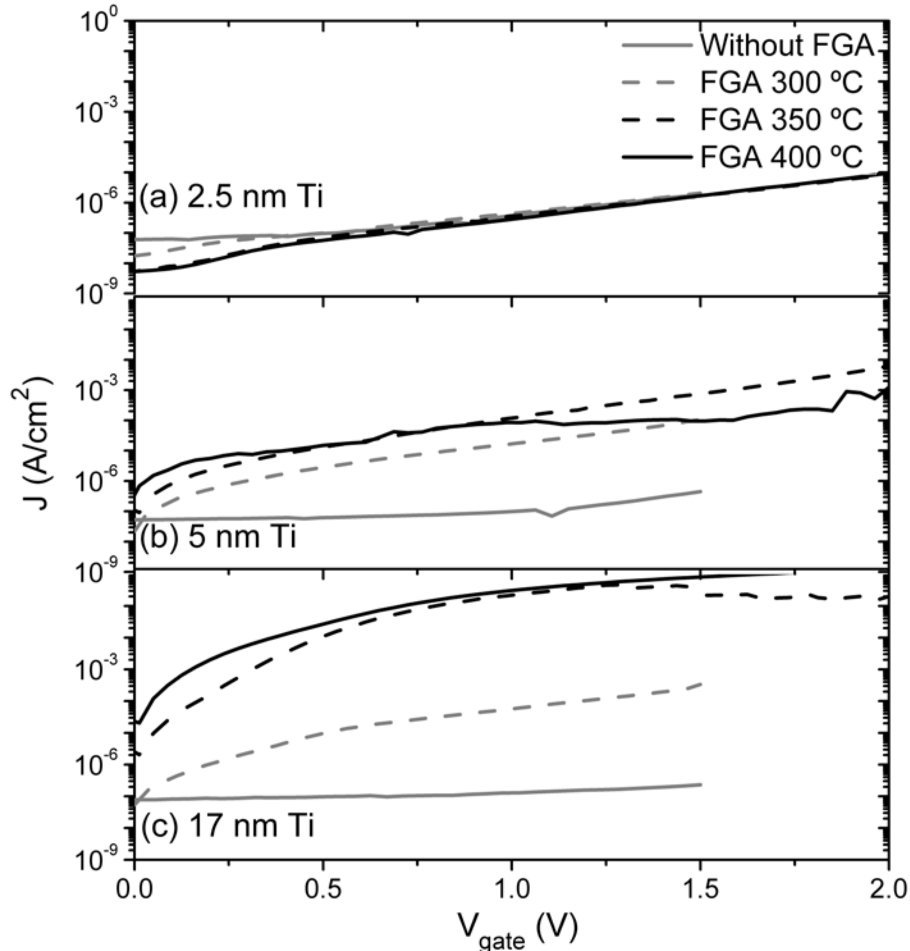

Figure VII.5: J-V_{gate} curves for the sample with 80 s of Gd and 100 s plasma oxidation at 20 W measured before and after several FGAs with different thickness of Ti layers: (a) 2.5 nm, (b) 5 nm and (c) 17 nm.

with 17 nm of Ti, the current density reaches a high value over 10^{-1} A/cm^2 at 1 V after the FGA at 350 °C as can be observed in figure VII.5(c). This confirms, again, that there is excessive scavenging in this sample. In any case, when comparing with the same SiO_2 dielectric thickness film of 1.2 nm [21], much lower values (more than four orders of magnitude lower) were obtained with this Gd_2O_3 layer.

Summarizing these results, 5 nm of Ti together with FGA at 300 °C is the best compromise between scavenging, D_{it} and leakage current. However, more intense scavenging should not be completely discarded, but it would require a metal gate-last process. In other words, after the FGA, the Ti gate should be substituted by a threshold voltage (V_T) control metal followed by an interface improvement process (for instance, FGA at 500 °C during 20 min).

The 5 nm Ti sample after the FGA at 400 ºC was further analyzed. First of all, DLTS measurements give a D_{it} value around 10^{12} eV^{-1}cm^{-2}, uniform through the gap (as it is presented in figure VII.6). These results are in good agreement with the values provided by the conductance method and presented in the right hand side of figure VII.4.

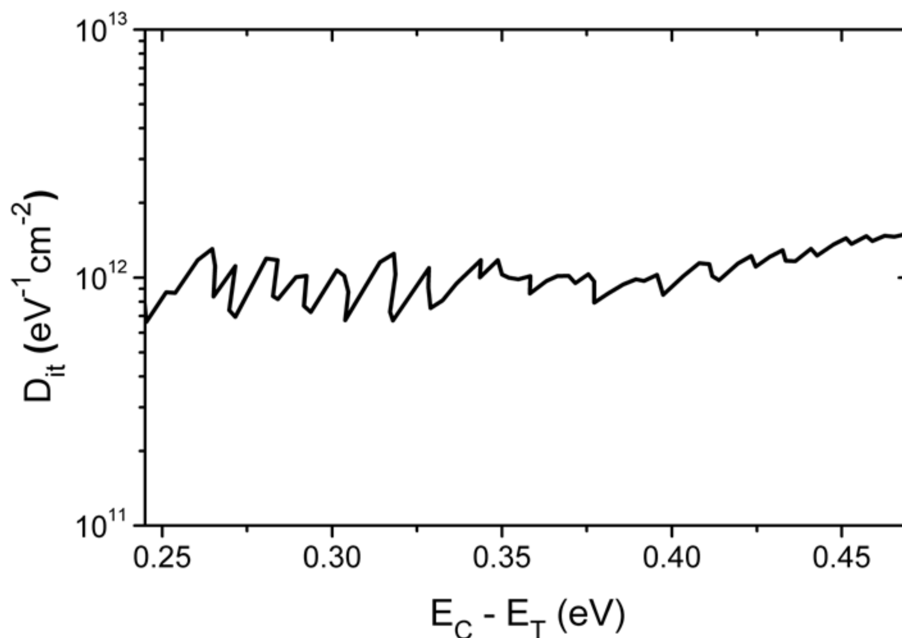

Figure VII.6: Interface trap density obtained by DLTS for sample with 80 s of Gd and 100 s oxidation at 20 W with 5 nm of Ti measured after the FGA at 400 ºC.

J-V_{gate} curves at different temperatures are obtained to characterize the leakage current density conduction mechanism. In figure VII.7(a), two regions can be distinguished. At low voltages ($V_{gate} < 0.1$ V), current density does not depend on the temperature. Therefore, tunneling is the dominant conduction mechanism in this region [22]. In contrast, for higher voltages, current is thermally activated. This dependency fits well to the Poole-Frenkel effect, that is, trap assisted conduction mechanism is dominant at electric field, E, values higher than 0.7 MV/cm. Figure VII.7(b) shows the plot of J/E (in logarithmic scale) against $E^{1/2}$ at several temperatures, corresponding to this sample with 5 nm of Ti layer and after the FGA at 400 °C. There is a linear dependence in the high-field range, as required by the Poole-Frenkel equation [23]:

$$I = I_0 exp\left(\frac{\beta_{PF} E^{1/2}}{kT}\right) E \qquad \textbf{(VII.1)}$$

where I is the current, I_0, a pre-exponential factor, β_{PF} is the Poole-Frenkel coefficient, E, the applied electric field, k is the Boltzmann's constant and T, the temperature. The obtained value of β_{PF} in the 0.7-1 MV/cm electric field range slightly varies with

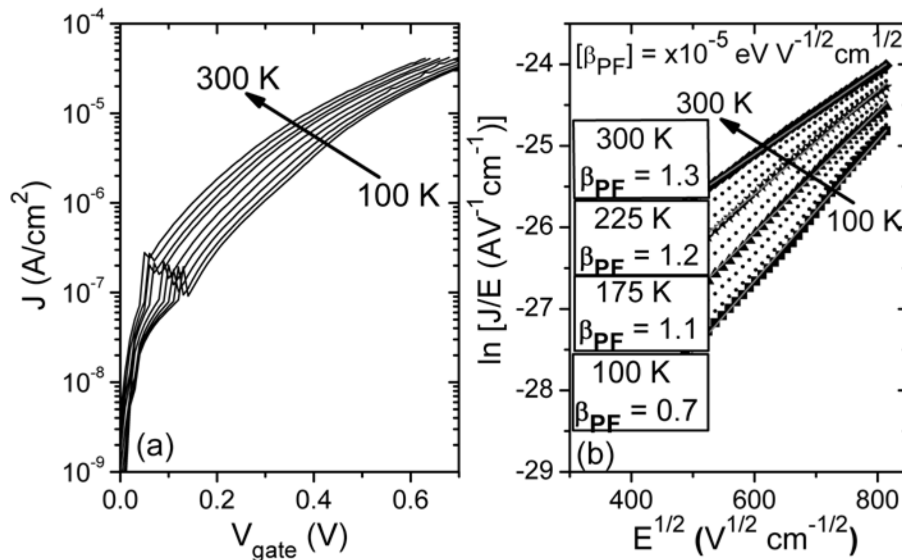

Figure VII.7: (a) J-V_{gate} characteristics measured at different temperatures (from 100 K to 300 K) and (b) current electric field dependency fitting following the Poole-Frenkel model at several temperatures for the Si sample with 5 nm of Ti and after the FGA at 400 °C. The β_{PF} parameter is shown in the figure.

temperature in the range (0.7-1.3)×10^{-5} eVcm$^{1/2}$V$^{-1/2}$. Similar values were obtained in different MIS samples with Gd_2O_3 fabricated with the same method [24].

To complete the electrical study, the frequency dispersion of the C-V_{gate} curves for this Ti sample annealing at 400 °C is shown in the left hand side of figure VII.8. All measured frequencies (from 1 kHz to 1 MHz) present almost the same value of the accumulation capacitance, except the one at 1 MHz, which is around 10% lower than the others. This reduction in the capacitance is due to combined effect of the series resistance with a high conductance (over ~1 S/cm^2 at gate voltages above 0 V) measured at this high frequency. Similar results were obtained for the Pt sample (presented in figure V.29). The hump of the C-V_{gate} curve in depletion due to the interface traps decreases when increasing frequency. The D_{it} values obtained from this figure by using the conductance method decrease almost one order of magnitude as the frequency is increased (from 2×10^{12} to 4×10^{11} eV^{-1}cm^{-2}). This means that most of the traps can follow the *ac* signal even at moderately high frequencies. The same behavior in similar samples but using pure Pt as top metal was observed previously in chapter V. This can be related to the existence of a border trap distribution inside the dielectric. As border traps are located further away from the interface, emission and capture time

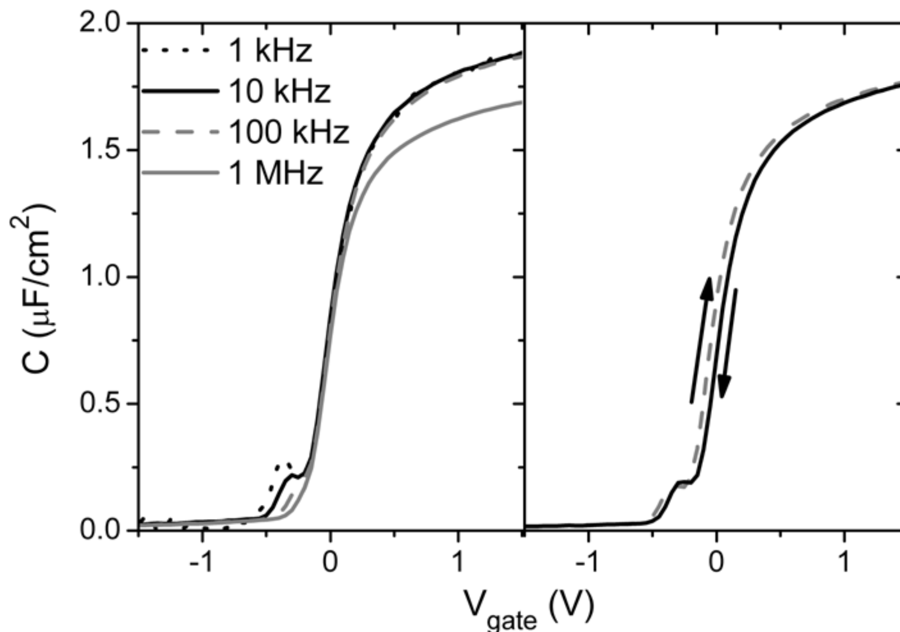

Figure VII.8: C-V_{gate} frequency dispersion curves measured from 1 kHz to 1 MHz (left) and hysteresis measured at 10 kHz (right) for the sample fabricated with 5 nm of Ti and after the FGA at 400 ºC.

constants exponentially decrease with the distance from the interface [25]. Therefore, only traps at the interface contribute to conductance values at high frequency.

The C-V_{gate} hysteresis characteristic measured at 10 kHz is presented in the right hand side of figure VII.8 after the FGA at 400 °C. The curve is obtained from inversion to accumulation and back again. The flatband voltage (V_{FB}) shift is around 56 mV. These results are similar to other works reported [18,26] and to that obtained for the Pt sample in chapter V (and shown in figure V.28(a)). This indicates that the FGA passivates most of the defects inside the Gd_2O_3 film that act as slow traps.

As a conclusion of this section, the choice of a proper thickness of the Ti layer (5 nm) enables the reduction of the interfacial oxide without compromising the leakage and the performance of the devices. Admissible values for the current density and the D_{it} are achieved for samples with an EOT of around 1.2 nm.

2.3.- Scavenging effect for plasma oxidized Sc_2O_3

Once it has been proved that the scavenging effect was compatible with Gd_2O_3 films and that this effect could be controlled with the thickness of the Ti overlayer and the annealing temperature, in this section, the compatibility of the scavenging effect was studied using MIS devices with Sc_2O_3. These MIS capacitors were fabricated with FOX and with 80 s of Sc and a plasma oxidation of 100 s (performed at 20 W). With these conditions, it was shown (in figure V.32) that the dielectric thickness was around 3.6 nm, much lower than in the Gd case. Therefore, in order to control the scavenging effect, 5 nm of Ti (capped with Pt) was used as top electrode.

Figure VII.9 depicted the area normalized capacitance as a function of the gate voltage for the Sc_2O_3 devices before (left) and after the FGA at 300 ºC (right) for the Ti capacitors (in black). It is also presented the Pt devices (in grey) as a reference. The as deposited capacitors with Ti show an important increase in the accumulation capacitance value compared to the Pt one (from ~1.8 to ~2.4 µF/cm^2), as it can be observed in the left hand side of this figure. Thus, in this case, the scavenging effect produced during the Ti e-beam evaporation is more intense than in the Gd_2O_3 case. After the FGA at 300 ºC, a capacitance roll off is caused due to an aggressive scavenging produced in these samples. This effect is more significant than in the former

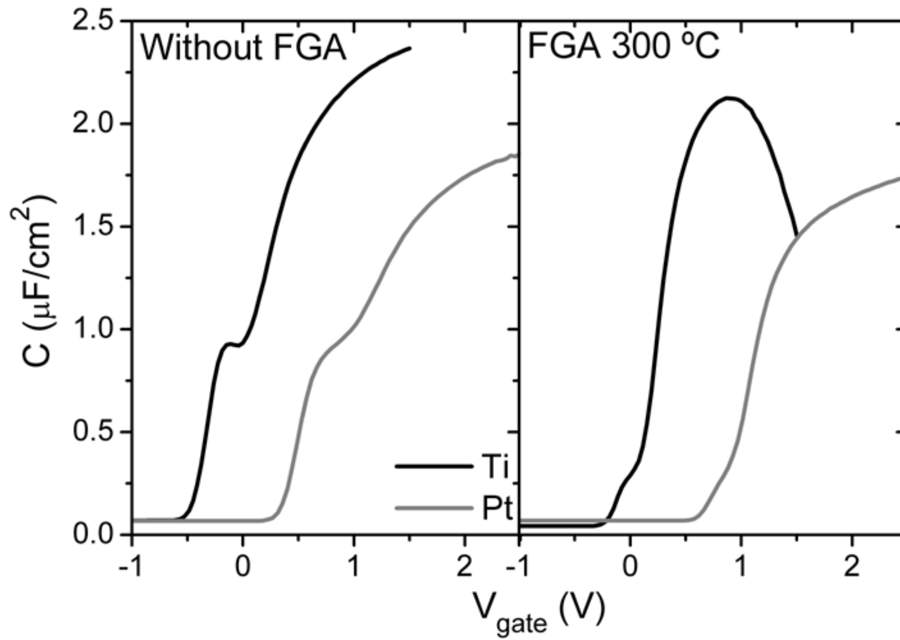

Figure VII.9: C-V_{gate} curves for the sample with 80 s of Sc and 100 s plasma oxidation at 20 W measured before (left) and after the FGA at 300 ºC (right) for two different electrodes: 5 nm of Ti capped with Pt (in black) and Pt (in grey as a reference).

section with Gd_2O_3. It is important to highlight that the thickness of the Sc_2O_3 film is only 3.6 nm (2.6 nm plus an interlayer of 1.0 nm) and, therefore, the conductance is high even for the as deposited sample when using 5 nm of Ti (this value is close to 2×10^{-1} S/cm^2 for V_{gate} higher than 1.5 V, more than one order of magnitude higher compared to the Pt sample, and increases to ~4 S/cm^2 after the FGA at 300 ºC).

Besides, in figure VII.9, there is a shift of the V_{FB} between the Ti electroded capacitor and the Pt one, before and after the FGA. Ideally, Ti should have a V_{FB} around 1 V lower than Pt [27], which is in good agreement with the results observed in this figure.

In table VII.2 is represented the EOT and the D_{it} values for both electrodes before and after the FGA at 300 ºC. The EOT is reduced 0.3 nm only by changing the top electrode from Pt to Ti, reaching a value of 1.2 nm, for the as deposited sample. After the FGA, due to the drop in the accumulation capacitance related to the high conductance, this value could not be obtained using [15]. In the case of the D_{it}, a slight reduction is achieved with the annealing, due to hydrogen passivation.

	Without FGA		FGA 300 ºC	
Metallic contact	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
Ti/Pt	1.2	5×10^{12}	---	1×10^{12}
Pt	1.5	4×10^{12}	1.6	7×10^{11}

Table VII.2: EOT and D_{it} values extracted from electrical measurements before and after the FGA at 300 ºC for samples with 80 s of Sc and a plasma oxidation of 100 s (at 20 W) with two different top electrodes: 5 nm of Ti capped with Pt and Pt layers.

The same effect commented before with the C-V_{gate} characteristics is observed in the current density, presented in figure VII.10: it increases its value around three orders of magnitude (from 10^{-4} to 10^{-1} A/cm^2 at 1.5 V) when changing the top electrode from Pt to Ti and before the FGA. Besides, the FGA at 300 ºC, increases up this value over 1 A/cm^2. In this case, the EOT of these samples is around (or lower than) 1.2 nm. There is uncertainty due to the capacitance roll off. MOS devices fabricated with this thickness of SiO_2 [21] presented values around two or three orders of magnitude higher.

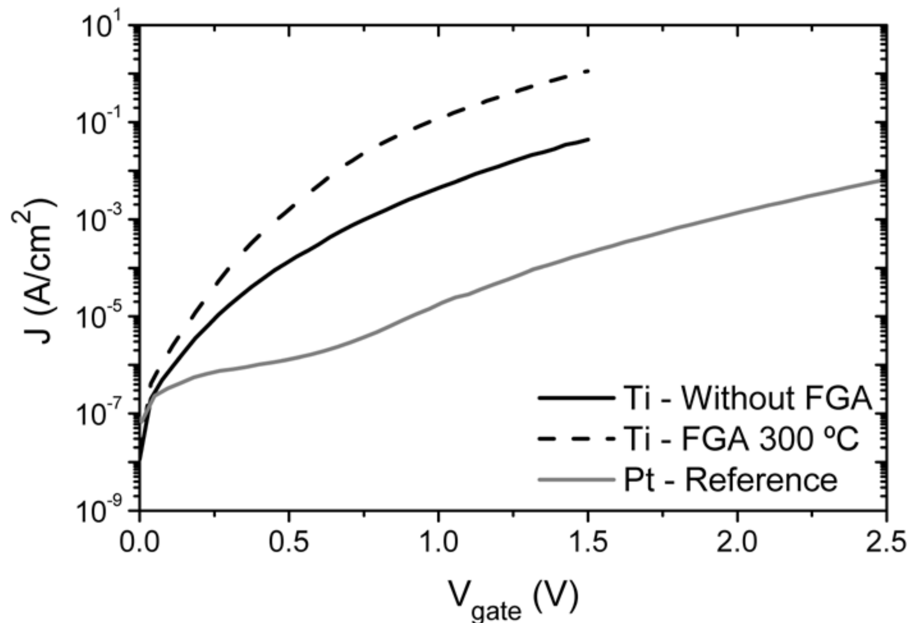

Figure VII.10: J-V_{gate} characteristics for the Sc_2O_3 sample (80 s of Sc and 100 s oxidation at 20 W) measured before (solid lines) and after the FGA at 300 ºC (dashed lines) for 5 nm of Ti capped with Pt (in black). As a reference, the Pt sample is represented in grey.

As a conclusion of this section, it had been proved that the scavenging effect is also compatible with Sc_2O_3 films grown with the two-step method. In fact, for these thin films scavenging was found even before performing the FGA because of the heating during e-beam evaporation. Due to the lower growth rate for this material, the control of the thickness of the Ti layer is very important for the proper device performance in order to have low leakage currents.

2.4.- Scavenging effect for plasma oxidized $Gd_{0.9}Sc_{1.1}O_3$

Finally, the scavenging effect produced by Ti electrodes is studied for MIS devices (with FOX) grown with $Gd_{0.9}Sc_{1.1}O_3$ as dielectric. This high κ material was obtained from a nanolaminate of thin Gd and Sc layers followed by a plasma oxidation (the same samples of chapter VI). As it was commented in the former chapter, the gadolinium scandate need a temperature treatment to mix the nanolaminate and form a homogeneous layer of 5.0 nm thick with 0.9 nm of IL (shown in figure VI.15). Therefore, the Ti layer (with a thickness of 5 nm) was evaporated after a FGA of the $Gd_{0.9}Sc_{1.1}O_3$ at 600 ºC during 5 min, in order to obtain a mixed layer and to ensure the formation of the gadolinium scandate before the scavenging process. After Ti evaporation to improve the metallic contacts and produce scavenging, a FGA at 300 ºC for 20 min was performed. The devices were measured before and after this second FGA.

In figure VII.11 is represented the area normalized capacitance as a function of the gate voltage for the capacitors with $Gd_{0.9}Sc_{1.1}O_3$ as dielectric. The Ti devices (in black) after the FGA at 600 ºC but before the FGA at 300 ºC (solid line) present a significant increase in the accumulation capacitance compared to the Pt samples after the FGA at 600 ºC (shown as a reference in grey) from 1.9 to ~2.2 $\mu F/cm^2$. Again, this increase is due to the scavenging effect produced during the Ti evaporation, as it was also observed for the other dielectrics analyzed in this chapter. It is important to remember that in these devices, the IL is only 0.9 nm thick and thus, a small reduction in the thickness of this layer would clearly increase the capacitance. Besides, a proper election of the Ti thickness is desirable, aiming of the absence of degradation of the dielectric. Additionally, a slight accumulation capacitance roll off is observed for this Ti

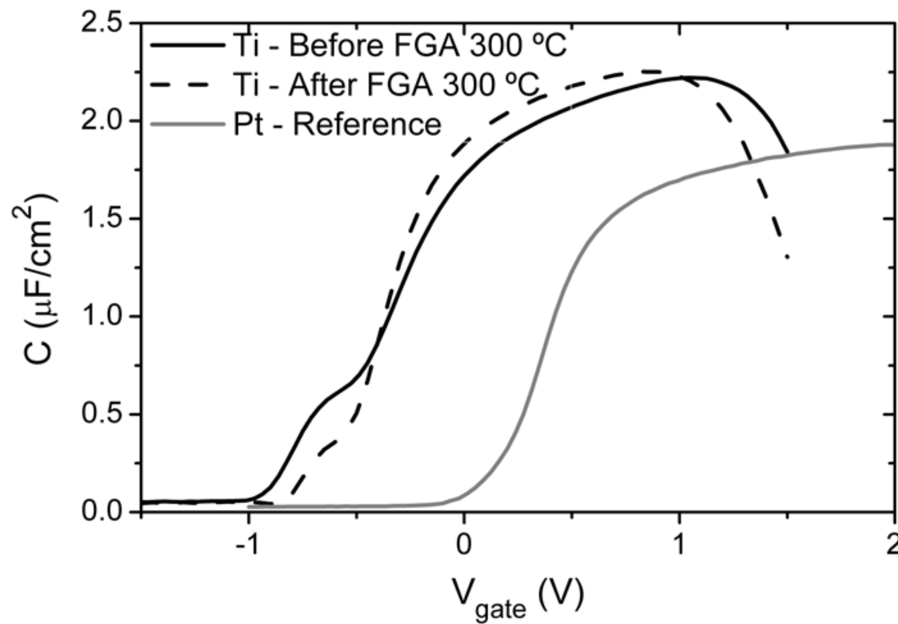

Figure VII.11: C-V_{gate} characteristics of capacitors with $Gd_{0.9}Sc_{1.1}O_3$ formed after a FGA at 600 ºC using Ti as top electrode (in black) before (solid line) and after a second FGA at 300 ºC (dashed line). The same dielectric with Pt is represented as a reference in grey.

sample for $V_{gate} > 1.0$ V, which is related to a high normalized conductance, that is higher than 2×10^{-1} S/cm^2, two orders of magnitude higher than in the Pt case.

Besides, a shift of around 1 V is observed in the V_{FB} for the Pt and Ti samples which is in accordance with the theory [27].

The impact of performing the second FGA at 300 ºC (represented in black dashed line) does not evidently change the accumulation capacitance. The EOT value is around 1.2 nm for the Ti sample before and after annealing. Due to the capacitance roll off, it is difficult to obtain the value after the FGA. However, it seems that the EOT decreases slightly after the second FGA at 300 ºC due to the scavenging effect. Remember that the Pt sample presented an EOT of 1.5 nm. Thus, the scavenging effect is significant when changing the top electrode.

Furthermore, the D_{it} is high (~10^{13} eV^{-1}cm^{-2}) for the Ti devices before and after the second FGA due to the formation of extra dangling bonds at the dielectric/Si interface, as it was commented before and was also reported in other work [16] related to the scavenging effect. This value is almost two orders of magnitude higher than the

Pt case, which was in the 10^{11} $eV^{-1}cm^{-2}$ range. However, performing the second FGA seems to improve the D_{it}, since the hump in depletion is smaller and the C-V_{gate} curve presents less stretch-out. These two effects are related to a lower D_{it}, as it was stated in chapter III.

Figure VII.12 depicts the leakage current density versus gate voltage characteristics for the devices with $Gd_{0.9}Sc_{1.1}O_3$. The same effects mentioned in the former paragraphs are observed in this figure. The Ti sample before the second FGA increases the leakage current around two orders of magnitude with respect to the Pt device (~6×10^{-1} and ~3×10^{-3} A/cm^2, respectively, at 1.5 V). This is related to the accumulation capacitance increase due to the scavenging effect produced by the Ti evaporation. Performing a second FGA at 300 ºC, slightly increase the current density to a value over 1 A/cm^2, which is a confirmation that there is some further scavenging during this FGA promoted by the temperature. However, comparing these values with 1.2 nm of SiO_2 [21], the leakage current density for this $Gd_{0.9}Sc_{1.1}O_3$ layer is much lower than that obtained for SiO_2.

The main conclusion of this section is that the compatibility of the scavenging effect has been demonstrated with gadolinium scandate formed by our optimized

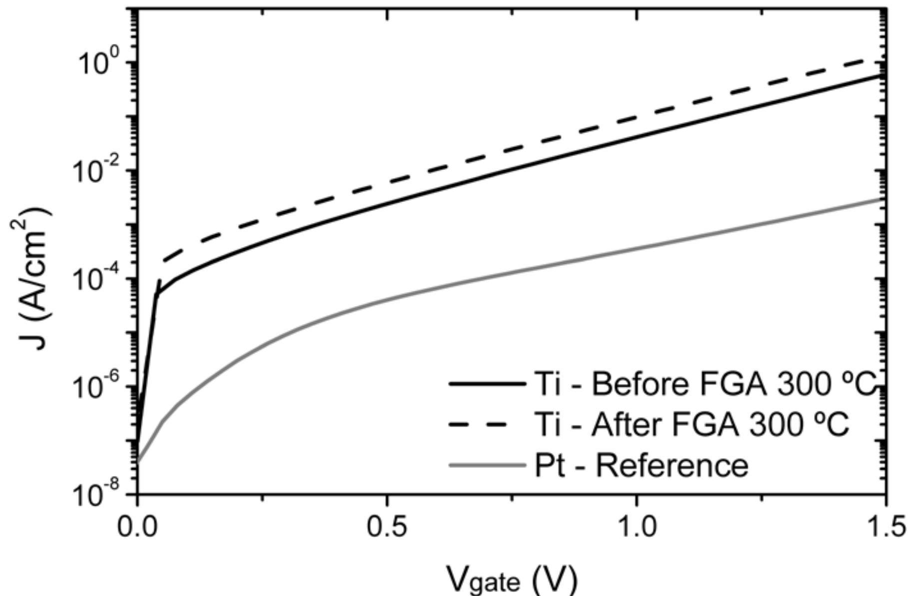

Figure VII.12: J-V_{gate} curves for the $Gd_{0.9}Sc_{1.1}O_3$ sample formed after a FGA at 600 ºC measured before (solid line) and after a second FGA at 300 ºC (dashed line) with 5 nm of Ti capped with Pt (in black). As a reference, the Pt sample is represented in grey.

two-step HPS process. An increase in the accumulation capacitance is achieved after the evaporation of the Ti metallic contact, accompanied by a reduction in the EOT of around 0.3 nm. Due to the lower IL thickness of these samples compared to the Gd_2O_3 devices, the scavenging effect is more significant and a proper election of the Ti thickness is critical to achieve a reduction of the SiO_x layer without compromising the dielectric quality.

VII.3.- SUMMARY AND CONCLUSIONS

In this chapter, the scavenging effect has been proved with MIS capacitors grown with Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ as dielectrics and using Ti as metallic electrode. For these three high κ materials, a clear increase in the accumulation capacitance was achieved. Therefore, a decrease in the EOT value was obtained. This effect was noticeable even before the temperature treatment, due to the infrared radiation produced during the Ti evaporation.

A suitable choice of the Ti overlayer thickness and the FGA temperature is crucial in order to achieve the desirable scavenging effect. This means a decrease of the SiO_x IL, accompanied by a lower EOT value but without degrading the dielectric material or compromising the electrical behavior of the MIS devices.

For the $Gd_{0.9}Sc_{1.1}O_3$ samples, the minimum EOT obtained with Ti is 1.2 nm, 0.3 nm lower than in the Pt case. This reduction is followed by an increase in the D_{it} and in the leakage current density, thus, a moderate degradation of the high κ material. One solution to control this would be to reduce the Ti thickness. In any case, from a production point of view after a controlled scavenging process that optimizes the EOT value, the Ti scavenging gate should be removed and replaced by other metallic stack followed by a FGA to passivate the interfacial defects in a gate-last process [28].

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